AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings of claims in the application:

1. (Currently Amended) A method to control the loading of a memory buffer, the memory buffer having a watermark with a first watermark value, the method comprising:

receiving an advance indication of a memory service interruption by a memory controller, wherein the received advance indication occurs prior to ~~a~~ the memory service interruption; and

based at least in part on the received advance indication of the memory service interruption, modifying the watermark to have a second watermark value different from the first watermark value.

2. (Original) The method of claim 1, wherein the memory buffer having a watermark has a below-watermark burst size with a first burst size value, the method further comprising:

based at least in part on the received advance indication of the memory service interruption, modifying the below-watermark burst size to have a second burst size value different from the first burst size value.

3. (Original) The method of claim 1, wherein the indication of a memory service interruption includes an advance indication of a memory service interruption having a worst case latency to memory.

4. (Original) The method of claim 1, wherein the second watermark value is greater than the first watermark value.

5. (Original) The method of claim 2 wherein the second burst size value is less than the first burst size value.

6. (Original) The method of claim 2 wherein the second burst size value corresponds to difference between the number of data entries in the memory buffer and the second watermark value.

7. (Original) The method of claim 1, the method further comprising

receiving an indication of the termination of the memory service interruption; and

based at least in part on the received indication of the termination of the memory service interruption, modifying the watermark to have a third watermark value different from the second watermark value.

8. (Original) The method of claim 7, wherein the third watermark value equals the first watermark value.

9. (Original) The method of claim 2, the method further comprising

receiving an indication of the termination of the memory service interruption;

based at least in part on the received indication of the termination of the memory service interruption, modifying the watermark to have a third value different from the second watermark value; and

based at least in part on the received indication of the termination of the memory service interruption, modifying the below-watermark burst size to have a third burst size value different from the second burst size value.

10. (Original) The method of claim 9, wherein the third watermark value equals the first watermark value, and wherein the third burst size value equals the first burst size value.

11. (Previously Amended) A method to control the loading of a memory buffer, the memory buffer having a watermark with a first watermark value, the method comprising:

modifying the watermark based at least in part on the received advance indication by a memory controller of a memory service interruption, wherein the received advance indication occurs prior to the memory service interruption, to have a second watermark value, the second watermark value being different than the first watermark value; and

modifying the watermark to have a third watermark value subsequent to the occurrence of the memory service interruption, the third watermark value being different than the second watermark value.

12. (Original) The method of claim 11, wherein the third watermark value equals the first watermark value.

13. (Previously Amended) The method of claim 11, wherein the memory buffer having a watermark with a first watermark value has an below-watermark burst size with a first burst size value, the method further comprising:

modifying the below-watermark burst size to have a second burst size value prior to the occurrence of a memory service interruption, the second burst size value being different than the first burst size value; and

modifying the below-watermark burst size to have a third burst size value subsequent to the occurrence of the memory service interruption, the third burst size value being different than the second burst size value.

14. (Original) The method of claim 13, wherein the first burst size value is equal to the third burst size value.

15. (Currently Amended) An apparatus to control the loading of a memory buffer, comprising:

a memory buffer; and

a memory controller to receive an advance indication of a memory service interruption, coupled to said memory buffer, including

a watermark register;

a first register, coupled to said watermark register, to store a first watermark value; and

a second register, coupled to said watermark register, to store a second watermark value.

16. (Original) The apparatus of claim 15, wherein the memory controller includes:

a below-watermark burst size register;

a third register, coupled to said below-watermark burst size register, to store a first below-watermark burst size value; and

a fourth register, coupled to said below-watermark burst size register, to store a second below-watermark burst size value.

17. (Currently Amended) The apparatus of claim 15, wherein the memory controller is to:

~~receive an advance indication of a memory service interruption;~~

read the second watermark value from said second register based at least in part on

the received advance indication of a memory service interruption; and

store the second watermark value in said watermark register.

18. (Currently Amended) The apparatus of claim 16, wherein the memory controller is to

~~receive an advance indication of a memory service interruption;~~

read the second watermark value from said second register based at least in part on the received advance indication of a memory service interruption; and

store the second watermark value in said watermark register:

read the second below-watermark burst size value from said fourth register based at least in part on the received advanced indication of a memory service interruption; and

store the second below-watermark burst size value in said below-watermark burst size register.

19. (Currently Amended) A system to process video signals, the system comprising:

a processor;

a memory, coupled to said processor;

a memory buffer, coupled to said memory; and

a memory controller to receive an advance indication of a memory service interruption, coupled to said memory buffer, including

a watermark register;

a first register, coupled to said watermark register, to store a first watermark value; and

a second register, coupled to said watermark register, to store a second watermark value.

20. (Currently Amended) The system of claim 19, wherein the memory controller is to:

~~receive an advance indication of a memory service interruption;~~

read the second watermark value from said second register based at least in part on the received advance indication of a memory service interruption; and

store the second watermark value in said watermark register.

21. (Currently Amended) A computer-readable medium storing a plurality of instructions to be executed by a processor to control a memory buffer having a watermark with a first watermark value and a below-watermark burst size with a first burst size value, said plurality of instructions comprising instructions to:

receive an advance indication of a memory service interruption by a memory controller, wherein the received advance indication is to occur prior to ~~a~~ the memory service interruption; and

based at least in part on the received advance indication of the memory service interruption, modify the watermark to have a second watermark value different from the first watermark value.

22. (Original) The computer-readable medium of claim 21, further comprising instruction to:

based at least in part on the received advance indication of the memory service interruption, modify the below-watermark burst size to have a second burst size value different from the first burst size value.

23. (Previously Added) An apparatus comprising:

a memory buffer; and

a memory controller coupled to said memory buffer, said memory controller to operate in a first mode maintaining a first level of buffering in said memory buffer and to switch to a second mode maintaining a second level of buffering that is higher than the first level of buffering in response to an advance indication of a memory service interruption.

24. (Previously Added) The apparatus of claim 23 wherein said memory service interruption is a DRAM refresh operation.

25. (Previously Added) The apparatus of claim 23 wherein said memory service interruption is a memory maintenance operation.

26. (Previously Added) The apparatus of claim 23 wherein said first mode has an associated first burst size and said second mode has an associated second burst size.

27. (Previously Added) The apparatus of claim 23 wherein said memory buffer is a video buffer to buffer a video stream retrieved from memory.

28. (Previously Added) An apparatus comprising:

a video stream buffer;

a memory controller to occasionally perform an operation causing a memory service interruption; and

control logic coupled to said video stream buffer to maintain a first level of buffering in a first mode and to maintain a higher level of buffering prior to said memory controller performing said operation causing said memory service interruption.

29. (Previously Added) The apparatus of claim 28 wherein said operation is a DRAM refresh operation.

30. (Previously Added) The apparatus of claim 29 further comprising a processor, wherein said processor, said video stream buffer, said memory controller, and said control logic are all integrated into a single integrated circuit.